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Method Of Forming Non-Volatile Resistance Variable Devices, Method Of Precluding Diffusion Of A Metal Into Adjacent Chalcogenide Material, And Non-Volatile Resistance Variable Devices

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Method Of Forming Non-Volatile Resistance Variable Devices, Method Of Precluding Diffusion Of A Metal Into Adjacent Chalcogenide Material, And Non-Volatile Resistance Variable Devices

TECHNICAL FIELD

This invention relates to non-volatile resistance variable devices and methods of forming the same, and to methods of precluding diffusion of a metal into adjacent chalcogenide material.

BACKGROUND OF THE INVENTION

Semiconductor fabrication continues to strive to make individual electronic components smaller and smaller, resulting in ever denser integrated circuitry. One type of integrated circuitry comprises memory circuitry where information is stored in the form of binary data. The circuitry can be fabricated such that the data is volatile or non-volatile. Volatile storing memory devices result in loss of data when power is interrupted. Non-volatile memory circuitry retains the stored data even when power is interrupted.

This invention was principally motivated in making improvements to the design and operation of memory circuitry disclosed in the Kozicki et al. U.S. Patent Nos. 5,761,115; 5,896,312; 5,914,893; and 6,084,796, which ultimately resulted from U.S. Patent Application Serial No. 08/652,706, filed on May 30, 1996, disclosing what is referred to as a programmable metalization cell. Such a cell includes opposing electrodes having an insulating dielectric

material received therebetween. Received within the dielectric material is a fast ion conductor material. The resistance of such material can be changed between highly insulative and highly conductive states. In its normal high resistive state, to perform a write operation, a voltage potential is applied to a certain one of the electrodes, with the other of the electrode being held at zero voltage or ground. The electrode having the voltage applied thereto functions as an anode, while the electrode held at zero or ground functions as a cathode. The nature of the fast ion conductor material is such that it undergoes a chemical and structural change at a certain applied voltage. Specifically, at some suitable threshold voltage, plating of metal from metal ions within the material begins to occur on the cathode and grows or progresses through the fast ion conductor toward the other anode electrode. With such voltage continued to be applied, the process continues until a single conductive dendrite or filament extends between the electrodes, effectively interconnecting the top and bottom electrodes to electrically short them together.

Once this occurs, dendrite growth stops, and is retained when the voltage potentials are removed. Such can effectively result in the resistance of the mass of fast ion conductor material between electrodes dropping by a factor of 1,000. Such material can be returned to its highly resistive state by reversing the voltage potential between the anode and cathode, whereby the filament disappears. Again, the highly resistive state is maintained once the reverse voltage potentials are removed. Accordingly, such a device can, for example, function as a programmable memory cell of memory circuitry.

The preferred resistance variable material received between the electrodes typically and preferably comprises a chalcogenide material having metal ions diffused therein. A specific example is germanium selenide having silver ions diffused therein. The present method of providing the silver ions within the germanium selenide material is to initially chemical vapor deposit the germanium selenide glass without any silver being received therein. A thin layer of silver is thereafter deposited upon the glass, for example by physical vapor deposition or other technique. An exemplary thickness is 200 Angstroms or less. The layer of silver is irradiated, preferably with electromagnetic energy at a wavelength less than 500 nanometers. The thin nature of the deposited silver enables such energy to pass through the silver to the silver/glass interface effective to break a chalcogenide bond of the chalcogenide material, thereby effecting dissolution of silver into the germanium selenide glass. The applied energy and overlying silver result in the silver migrating into the glass layer such that a homogenous distribution of silver throughout the layer is ultimately achieved.

Saturation of silver in germanium selenide is apparently at about 35 atomic percent. Yet, preferred existing technology for cell fabrication constitutes a concentration which is less than 35%, for example 27%. By controlling the time of irradiation, the quantity of silver provided within the glass can be desirably controlled to some suitable percent below saturation.

However, once the desired irradiation of the silver/glass composite is completed to achieve the desired silver incorporation, the wavelength of radiation required for further dissolution of the silver greatly reduces, even

lowering to that of standard room lighting. This is due to the band gap of the underlying material shifting with increasing silver incorporation. Further, and regardless, the substrate is almost invariably next subjected to photolithographic processing resulting in exposure to actinic energy at wavelengths above standard room lighting, which can undesirably cause more silver to be incorporated into the glass than the desired amount.

It would be desirable to develop ways to prevent or at least reduce this additional undesired silver incorporation into the resistance setable material. While the invention was principally motivated in achieving this objective, it is in no way so limited. The artisan will appreciate applicability of the invention in other aspects of processing involving chalcogenide materials, with the invention only being limited by the accompanying claims as literally worded and as appropriately interpreted in accordance with the doctrine of equivalents.

SUMMARY

The invention includes non-volatile resistance variable devices and methods of forming the same, and methods of precluding diffusion of a metal into adjacent chalcogenide material. In one implementation, a method of precluding diffusion of a metal into adjacent chalcogenide material upon exposure to a quanta of actinic energy capable of causing diffusion of the metal into the chalcogenide material includes forming an actinic energy blocking material layer over the metal to a thickness of no greater than 500 Angstroms and subsequently exposing the actinic energy blocking material layer to said quanta of actinic energy. In one implementation, an homogenous actinic energy blocking material layer is formed over the metal and subsequently exposed to said quanta of actinic energy.

In one implementation, a method of forming a non-volatile resistance variable device includes providing conductive electrode material over chalcogenide material having metal ions diffused therein. An actinic energy blocking material layer is formed on the conductive electrode material, the actinic energy blocking material layer being effective to shield actinic energy from reaching an interface of the conductive electrode material and the actinic energy blocking material to substantially preclude diffusion of the conductive electrode material into the chalcogenide material upon exposure to said actinic energy. A dielectric layer is formed on the actinic energy blocking material layer. The conductive electrode material is formed into a first electrode. A second electrode is provided proximate the chalcogenide material having the metal diffused therein.

Other implementations and aspects are contemplated and disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment 10 is shown in but one preferred embodiment of a method of forming a non-volatile resistance variable device. By way of example only, example such devices include programmable metalization cells and programmable optical elements of the patents referred to above, further by way of example only, including programmable capacitance elements, programmable resistance elements, programmable antifuses of integrated circuitry and programmable memory cells of memory circuitry. The above patents are herein incorporated by reference. The invention contemplates the fabrication techniques and structure of any existing non-volatile resistance variable device, as well as yet-to-be developed such devices. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Also in the context of this document, the term "layer" encompasses both the singular and the plural unless otherwise indicated. Further, it will be appreciated by the artisan that

"resistance setable semiconductive material" and "resistance variable device" includes materials and devices wherein a property or properties in addition to resistance is/are also varied. For example, and by way of example only, the material's capacitance and/or inductance might also be changed in addition to resistance.

Semiconductor wafer fragment 10 comprises a bulk monocrystalline semiconductive material 12, for example silicon, having an insulative dielectric layer 14, for example silicon dioxide, formed thereover. A conductive electrode material 16 is formed over dielectric layer 14. By way of example only, preferred materials include any of those described in the incorporated Kozicki et al. patents referred to above in conjunction with the preferred type of device being fabricated. A dielectric layer 18 is formed over first electrode 16. Silicon nitride is a preferred example.

An opening 20 is formed through layer 18 to conductive electrode layer 16. Such is filled with a chalcogenide material 22. Example and preferred materials are those disclosed in the Kozicki et al. patents above. Specifically, and by way of example only, preferred chalcogenide materials include Ge_xA_y, where "A" is selected from the group consisting of Se, Te and S, and mixtures thereof. An example preferred method of forming material 22 over substrate 10 is by chemical vapor deposition to completely fill opening 20, followed by a planarization technique, for example chemical-mechanical polishing. A metal, shown in the preferred embodiment in the form of a blanket layer 24, is formed over chalcogenide material 22. An example and preferred material for layer 24 is elemental silver. By way of

example only, example alternates include gold and copper, although copper is not expected to be usable in the context of the preferred Ge_xA_y programmable metalization cell being fabricated. Layer 24 is preferably deposited to a thickness at least one-third that of the thickness of chalcogenide material 22 received within opening 20.

Referring to Fig. 2, metal 24 is irradiated effective to break a chalcogenide bond of the chalcogenide material at an interface of metal 24 and chalcogenide material 22, and diffuse at least some of metal 24 into chalcogenide material 22. Material 22 is designated with numeral 23 and peppered in the drawings to indicate metal ions being received therein. A preferred irradiating includes exposure to actinic radiation having a wavelength below 500 nanometers, with radiation exposure at between 404-408 nanometers being a more specific example. A more specific example is a flood UV exposure tool operating at 4.5 milliwatts/cm^2 energy, for 15 minutes, in an oxygen containing ambient at room temperature and pressure.

All of material 24 received directly over chalcogenide material 22 might be diffused to within such material, or some portion thereof might remain as is shown. The thickness of layer 24 is also chosen to be suitably thin to enable the impinging electromagnetic radiation to essentially transparently pass through material 24 to the interface of such material with chalcogenide material 22. An example preferred range for the thickness of layer 24 is from about 140 Angstroms to about 200 Angstroms.

Referring to Fig. 3, after the irradiating, conductive electrode material 26 is formed over chalcogenide material 23 having the metal diffused

therein. An example preferred thickness range for electrode material 26 is from 140 Angstroms to 200 Angstroms. Layer 26 and any remnant metal 24 received directly over chalcogenide material 23 will constitute one electrode of the resistance variable device being fabricated, with layer 16 constituting another or second electrode for the device. In accordance with the preferred programmable metalization cell embodiment, at least one of electrode 26/24 and electrode 16 will constitute silver in contact with chalcogenide material 23. Example preferred materials for layer 26 include silver, tungsten and tungsten nitride. Further in the context of this document, any remnant material 24 received over chalcogenide material 23 will form a part of the upper electrode as shown, and accordingly, inherently constitutes conductive electrode material. Accordingly, in the illustrated Fig. 3 embodiment, conductive electrode material 24/26 received over chalcogenide material 23 constitutes two individual layers 24 and 26. In a preferred embodiment, both preferably comprise the same material, specifically silver, and particularly where lower electrode 16 comprises a material other than silver.

Referring to Fig. 4, an actinic energy blocking material layer 28 is formed on conductive electrode material 26/24. In the preferred embodiment, such material layer is effective to shield actinic energy from reaching the interface of materials 26/24 and chalcogenide material 23 to substantially preclude diffusion of metal 24 into chalcogenide material 23 upon exposure to said actinic energy. In one preferred embodiment, layer 28 is insulative. In another preferred embodiment, layer 28 is conductive, thereby forming a part of the illustrated upper electrode. Further in one embodiment, the actinic

energy blocking material is actinic energy reflective. In another preferred embodiment, the actinic energy blocking material is actinic energy absorptive and thereby antireflective. By way of example only, example conductive and reflective actinic energy blocking materials include tungsten and tungsten nitride. By way of example only, example actinic energy blocking materials which are both absorptive and insulative include amorphous silicon, silicon oxynitride, silicon-rich silicon nitride, and silicon-rich silicon dioxide.

In the preferred embodiment where a programmable metalization cell is being fabricated which comprises germanium selenide having silver therein, the deposition temperature for providing or otherwise forming layer 28 is preferably at or below 130°C. This is desirable to maintain the preferred embodiment germanium selenide material in a desired operative substantially amorphous state. Actinic energy blocking material 28 is preferably formed to a thickness no greater than 500 Angstroms, and preferably no thinner than 100 Angstroms. Further, actinic energy blocking layer 28 is preferably homogenous in composition, and constitutes a singular layer. Note also that the illustrated layer 26 might be fabricated to constitute an actinic energy blocking material (with or without additional layers) where at least some metal 24 remains over chalcogenide material 23 after the irradiating. In the preferred embodiment, the actinic energy blocking material layer enables the device to be subjected or otherwise exposed to actinic energy which would otherwise be effective to cause more diffusion of metal 24 into chalcogenide material 23, but which is substantially precluded by provision of the actinic energy blocking material.

Referring to Fig. 5, materials 28, 26 and 24 are patterned into an electrode 30. Where layer 28 constitutes conductive material, such forms a part of electrode 30. Where layer 28 comprises an insulative material, such effectively does not constitute a part of the conductive electrode 30, but rather constitutes an insulative material layer received thereover. Patterning to produce electrode 30 is typically and preferably conducted utilizing photolithography whereby actinic energy blocking material layer 28 is inherently exposed to actinic energy, with layer 28 substantially precluding further diffusion of metal layer 24 into chalcogenide material 23.

Referring to Fig. 6, one or more dielectric layers 32 are ultimately formed over actinic energy blocking material layer 28. Of course, intervening conductive and semiconductive layers might also be provided to form other lines and devices outwardly of the depicted device 30.

Independent of the method of fabrication, the invention comprises a non-volatile resistance variable device comprising some substrate having a first electrode formed thereover, for example either electrode 30 or electrode/layer 16. A resistance variable chalcogenide material 23 having metal ions diffused therein is received operatively adjacent the first electrode. A second electrode, for example the other of electrode 30 or electrode/layer 16, is received operatively adjacent the resistance variable chalcogenide material. In one embodiment, an actinic energy blocking material layer is received on the electrode to a thickness of no greater than 500 Angstroms. In one embodiment, a substantially homogenous actinic energy blocking material layer is received on the electrode independent of thickness.

Preferably, the actinic energy blocking material layer is both substantially homogenous and of a thickness no greater than 500 Angstroms. In the preferred embodiment, the device is configured as a programmable memory cell, for example the programmable metalization cell as described above.

The invention also constitutes a non-volatile resistance variable device independent of actinic energy blocking effects. In one implementation, such a device comprises a first layer of material which is received on the electrode to a thickness of no greater than 500 Angstroms, with such material being any one or combination of amorphous silicon, silicon oxynitride, silicon-rich silicon nitride, silicon-rich silicon dioxide, tungsten and tungsten nitride. In one embodiment, such a non-volatile resistance variable device comprises a first homogenous layer of material received on the electrode, with such material constituting one or more of amorphous silicon, silicon oxynitride, silicon-rich silicon nitride, silicon-rich silicon dioxide, tungsten and tungsten nitride.

Further, the invention, independent of the device being fabricated, comprises in one embodiment a method of precluding diffusion of a metal into adjacent chalcogenide material upon exposure to a quanta of actinic energy capable of causing diffusion of the metal into the chalcogenide material. In one implementation, such inventive method comprises forming an actinic energy blocking material layer over the metal to a thickness of no greater than 500 Angstroms and subsequently exposing the actinic energy blocking material layer to said quanta of actinic energy. In one implementation, such method includes forming a homogenous actinic energy

blocking material layer over the metal and subsequently exposing the actinic energy blocking material layer to said quanta of actinic energy. Most preferably, the actinic energy blocking material layer is both homogenous and provided to a thickness of no greater than 500 Angstroms.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.